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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/525,802	03/15/00	HIDAKA I	AKM-00301

EXAMINER	
CRUZ, L	
ART UNIT	**PAPER NUMBER**
2815	4

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PATENT GROUP
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

1- File Copy

PTO-90C (Rev. 2/95)

US GPO 2000; 465-188/25266

Office Action Summary	Application No.	Applicant(s)	
	09/525,802	HIDAKA, ITSUO	
	Examiner	Art Unit	
	Lourdes C. Cruz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *15 March 200* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☒ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

This Office Action is in response to an application filed March 15, 2000.

Drawings

Figures 8 and 9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Landis (U.S. Patent No. 4673904).

Landis discloses a semiconductor device (See Fig. 8) having multiple wiring layers, comprising: a signal line (84), which is formed in a wiring layer, and to which a signal voltage is applied;

two adjacent lines (80) which are so adjacent to said signal line as not to be connected thereto, and which are formed in a wiring layer where said signal line is formed.

two intersection lines (90,68) which are respectively formed in wiring layers each being present via an insulating layer (70) above or under the wiring layer where said signal line and said adjacent line are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines.

a plurality of entire-line-area through holes (88,86,74,72) which respectively penetrate through the insulating layers formed between said adjacent lines, and which respectively and electrically connect said two adjacent lines and said two intersection lines.

Regarding claim 2, Landis discloses the semiconductor device according to claim 1, wherein said two adjacent lines are formed substantially parallel to said signal line.

Claims 5-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Schreiber et al. (U.S. Patent No. 4845311).

With regard to claim 5, Schreiber et al. disclose a semiconductor device (See Fig. 1) having multiple wiring layers, comprising: a plurality of signal lines (60), which is formed not to intersect each other in an identical wiring layer;

two adjacent lines (44,42) which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto, and which are formed in a wiring layer where said plurality of signal lines is formed.

two intersection lines (74,76) which are formed in wiring layers each being present via an insulating layers (82) above or under the wiring layer where said signal line and said adjacent line are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and

a plurality of entire-line-area through holes (26,27) which respectively penetrate through the insulating layers formed between said adjacent lines, and which

respectively and electrically connect said two adjacent lines and said two intersection lines.

With regard to claim 8, Schreiber et al. disclose a semiconductor device (See Fig. 1) having multiple wiring layers, comprising: a plurality of signal lines (60), which are formed not to intersect each other in an identical wiring layer;

two first adjacent lines (44,42) which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto, and which are formed in a wiring layer where said plurality of signal lines is formed.

at least one second adjacent line (not labeled) which is formed in the wiring layer where said plurality of signal lines are formed, between said plurality of signal lines so as not to be connected to said plurality of signal lines;

two intersection lines (74,76) which are formed in wiring layers each being present via an insulating layers (82) above or under the wiring layer where said signal line and said adjacent line are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and

entire-line-area through holes (26,27) which respectively penetrate through the insulating layers (82) formed between said adjacent lines, and which respectively and electrically connect said two adjacent lines and said two intersection lines.

With regard to claim 10, Schreiber et al. discloses a semiconductor device (See Fig. 1) having multiple wiring layers, comprising: a plurality of signal lines (60), which are formed substantially in parallel to each other in different wiring layers;

a plurality of adjacent lines (44,42) each pair of which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto, and which are formed in a wiring layer where said plurality of signal lines is formed.

two intersection lines (74,76) each of which is formed in a layer under a lowermost wiring layer where plurality of signal lines are formed, and which are formed along a surface area corresponding to an area enclosed by said plurality of adjacent lines formed on the both extreme sides of said plurality of signal lines (See Fig. 1); and

a plurality of first entire-line-area through holes (26,17) which penetrate through an insulating layer (82) arranged between said adjacent lines (See Fig. 1), and which electrically connect said adjacent lines with said two intersection lines; and

a plurality of second entire-line-area through holes (27,19) which penetrate through an insulating layer arranged between said adjacent lines, along the entire areas of said adjacent lines, and which electrically connects said adjacent lines with each other (See Fig. 1).

With regard to claim 13, Schreiber et al. disclose a semiconductor device (See Fig. 1) having multiple wiring layers, comprising: a plurality of signal lines (60), which are formed in different wiring layers, and to which signal voltages are applied;

a plurality of adjacent lines (40,46) each pair of which are formed either in a lowermost or uppermost wiring layer, of the wiring layers where said plurality of signal lines (60) are formed, respectively adjacent onto both sides of one of said plurality of signal lines which is formed in an identical layer, thereby not to be connected to the one of said plurality of signal lines;.

two first intersection lines (Not labeled) each of which is formed either in a wiring layer under a lowermost wiring layer of said signal lines, or in a wiring wiring layer above the uppermost wiring layer of said signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said plurality of signal lines formed either in the lowermost or uppermost wiring layer of said signal lines (See Fig. 1);

a second intersection line (42) which is formed in a wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through holes (81,85) which penetrate through insulating layers between said adjacent lines (See Fig. 1) and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

a plurality of second entire-line-area through holes (17,27) which penetrate through insulating layers (82) formed between said adjacent lines and said second intersection lines, along the entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said intersection line (See Fig. 1).

Regarding claim 16, Schreiber et al. disclose the semiconductor device according to claim 13, wherein said signal lines are formed in different layers wich are adjacent to each other intersect each other.

Regarding claims 3-9,11,12 and 14,15,17 and 18 see In re Pearson 181 USPQ 641 (CCPA) which makes clear that terms merely setting forth intended use for, or a

property inherent in, an otherwise old composition do not differentiate claimed composition from those known to prior art. See also, In re Swinehart [169 USPQ 226] (CCPA 1971) which makes clear that mere recitation of a newly discovered function or property, inherently possessed by things in prior art, does not cause claim drawn to those things to distinguish over prior art.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kobayashi (U.S. Patent 5357138) discloses a coaxial wiring pattern structure in a multi layered wiring board. Tomie (U.S. Patent 6043556) discloses a high frequency input/output package. Tsuji (U.S. Patent No. 5491352) discloses a semiconductor device having peripheral metal wiring. Yamamoto et al. (U.S. Patent No. 4626889) disclose a stacked differentially driven transmission line on integrated circuit. Hesson et al. (U.S. Patent No. 5136357) disclose a low-noise, area efficient line structure. Cronin et al. (U.S. Patent No. 4776087) disclose a VLSI coaxial wiring structure. Latham, IV et al. (U.S. Patent No. 5811882) disclose on-chip shielding coaxial conductors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lourdes C. Cruz whose telephone number is 707-306-5691. The examiner can normally be reached on M-F 8:00- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mahshid D Saadat can be reached on 703-308-0956. The fax phone

numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Lourdes Cruz
June 16, 2000

Lourdes C. Cruz
Examiner
Art Unit 2815

DAVID HARDY
PRIMARY EXAMINER